For immediate Press Release

DefineView Consulting promotes System Verilog Assertions and higher levels of FPGA verification methodologies at the First Ever FPGA Summit.

What: FPGA Summit (http://www.fpgasummit.com)
Where: Wyndham Hotel, San Jose, Calif.
When: December 9-11, 2008

Los Gatos, Calif., Dec. 8, 2008 -- DefineView Consulting, provider of in-depth, application oriented training and consulting services in System Verilog Assertions, Functional Coverage, Assertion Based and Coverage Driven Verification methodologies will be participating in the FPGA Summit to promote the use of higher levels of Functional Verification Languages and Methodologies for FPGA Design community.

DefineView Consulting Booth:
DefineView will be showcasing advanced verification methodologies in their Booth (#1) on the FPGA Summit Exhibit floor.

Year-in-Review Panel Participation:
Ashok Mehta, founder of DefineView Consulting, will be participating in the Year-in-Review Panel on December 9th (5-7pm). He will discuss the role of System Verilog Assertions in FPGA design verification. The title of his presentation is "Get on with System Verilog Assertions for FPGA Design and Verification."

About The FPGA Summit
The FPGA Summit is the only practitioner-oriented conference dedicated entirely to FPGAs and their applications. It is intended for system designers, hardware and software engineers, product marketing and marketing communications specialists, test engineers and engineering and marketing managers. It features keynote, half-day tutorials, paper and panel sessions, and expert tables. Subjects include reconfigurable computing, communications/networking applications, DSP applications, verification, military/defense applications, low power design, computer applications, market research, design tips, testing and reliability, on-board processors and security. The Summit also includes exhibits of latest products. For more information, visit http://www.fpgasummit.com.

About DefineView Consulting
DefineView Consulting provides in-depth, application oriented training and consulting services in System Verilog Assertions, Functional Coverage and Constrained Random Verification Languages and Methodologies for ASIC and FPGA design verification.

Taught from real life experience at delivering first pass working designs, the training also includes a Reference Grade Training Book and practical LABs. Instructors are seasoned design/verification engineers with years of experience as end users of HDLs and HVLs.

Ashok Mehta, founder and principal instructor, has worked in the semiconductor industry for the past 25 years in hardware design and verification engineering and management positions at companies such as Digital, Intel, AMCC and many startups. He has extensive experience in design verification of complex SoC and Processor projects including the first Pentium's Architectural Verification project. Ashok has been a member of technical sub-committees on Verilog-SDF, and EIA 576.

For further information on training/consulting services, please visit http://www.defineview.com or send an email to info@defineview.com

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