
‘concurrent assertion’

it’s a vacuous world !

Concurrent Assertion - *without* an implication

Look! NO IMPLICATION

```
property pr1;  
  @(posedge clk) req ##2 gnt;  
endproperty
```

```
reqGnt: assert property (pr1) $display($stime,, "\t\t %m PASS"); else  
  $display($stime,, "\t\t %m FAIL");
```

Simulation Log

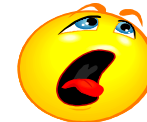
```
# run -all  
# 10 clk=1 req=0 gnt=0  
# 10 test_basic_property.reqGnt FAIL  
# 30 clk=1 req=0 gnt=0  
# 30 test_basic_property.reqGnt FAIL  
# 50 clk=1 req=1 gnt=0  
# 70 clk=1 req=0 gnt=0  
# 70 test_basic_property.reqGnt FAIL  
# 90 clk=1 req=0 gnt=1  
# 90 test_basic_property.reqGnt FAIL  
# 90 test_basic_property.reqGnt PASS  
# 110 clk=1 req=0 gnt=0  
# 110 test_basic_property.reqGnt FAIL
```

Whenever 'req' is Low, the assertion FAILs !!

That's because, a sequence simply says that 'req' be true at the clock edge and that gnt must be true 2 clocks later.

It does **NOT** say check the sequence "Only If 'req' is true at posedge clk".

But you really don't care for result when 'req' is Low.



That's where an implication operator comes into picture...

Concurrent Assertion - *with* an implication

```
sequence sr1;
##2 gnt;
endsequence

property pr1;
  @(posedge clk) req |-> sr1;
endproperty

reqGnt: assert property (pr1) $display($stime,, "\t\t %m PASS"); else
        $display($stime,, "\t\t %m FAIL");
```

Diagram illustrating the structure of the property assertion: **IMPLICATION OPERATOR (OVERLAPPING)** is shown above the property definition. Below it, **ANTECEDENT** points to the left side of the implication operator (`req`), and **CONSEQUENT** points to the right side (`sr1`).

Simulation Log

```
# 10 clk=1 req=0 gnt=0
# 10 test_basic_property1.reqGnt PASS
# 30 clk=1 req=1 gnt=0
# 50 clk=1 req=0 gnt=0
# 50 test_basic_property1.reqGnt PASS
# 70 clk=1 req=0 gnt=1
# 70 test_basic_property1.reqGnt PASS
# 70 test_basic_property1.reqGnt PASS
# 90 clk=1 req=1 gnt=0
# 110 clk=1 req=0 gnt=0
# 110 test_basic_property1.reqGnt PASS
# 130 clk=1 req=0 gnt=0
# 130 test_basic_property1.reqGnt FAIL
```

In this example, we moved a part of the sequence to the property and are using it as an antecedent to imply a consequent.

With an implication operator, the 'antecedent' MUST be TRUE to evaluate the consequent. Hence, whenever 'req' is Low, the antecedent is false and the implication simply does not fire and there is no failure message as in the previous example.

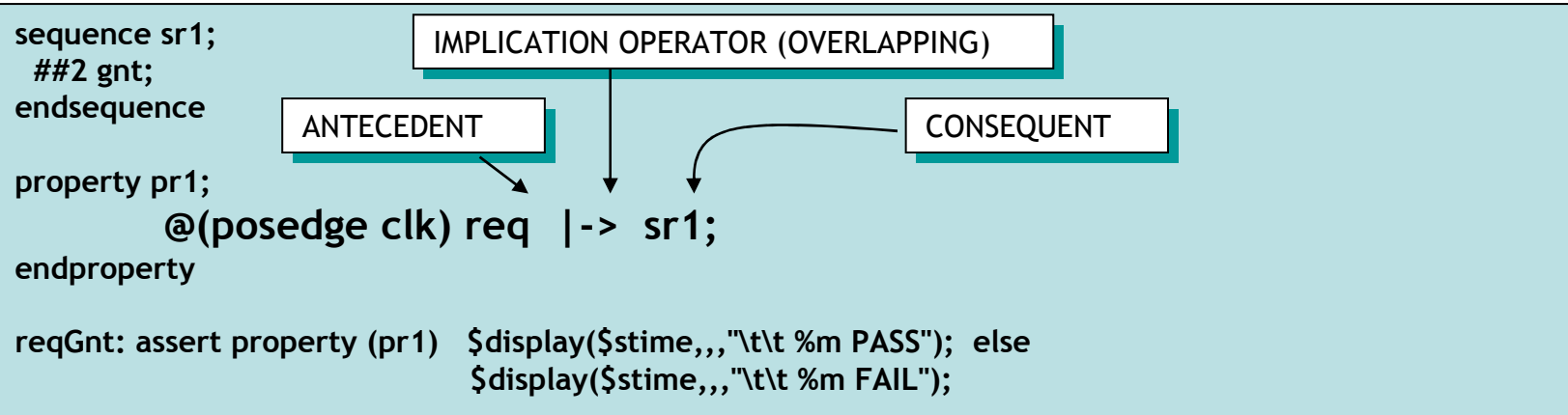
BUT WAIT...



Now the property PASSES whenever 'req' is Low.

What's going on???

Concurrent Assertion - *Vacuous Pass* - What ??



LRM 3.1a (Page 232) ::

“If there is no match of the antecedent sequence_expr, then evaluation of the implication succeeds vacuously and returns true”

A couple of ways to get around this...

One is to simply not use the action_block associated with ‘pass’ (duh...) of the property, so that you don’t get pass indication vacuously

But what if you do want to know when the property passes...

Concurrent Assertion - with 'cover'... take 1...

```
sequence sr1;
##2 gnt;
endsequence

property pr1;
@(posedge clk) req |-> sr1;
endproperty

A_reqGnt: assert property (pr1) else $display($stime,, "\t\t %m FAIL");

C_reqGnt: cover property (pr1) $display($stime,, "\t\t %m PASS");
```

IMPLICATION OPERATOR (OVERLAPPING)

ANTECEDENT

CONSEQUENT

No action_block associated with true eval of the property.

You may use a 'cover' statement to cover the same property that is asserted. 'cover' does not report vacuous pass (*but note that many simulators require a run time option to 'filter' out vacuous pass on a 'cover'*).

Note that 'cover' does not allow an action_block if the property fails.

```
# run -all
# 10 clk=1 req=0 gnt=0
# 30 clk=1 req=1 gnt=0
# 50 clk=1 req=0 gnt=0
# 70 clk=1 req=0 gnt=1
# 70 test_basic_property2.C_reqGnt PASS
# 90 clk=1 req=1 gnt=0
# 110 clk=1 req=0 gnt=0
# 130 clk=1 req=0 gnt=0
# 130 test_basic_property2.A_reqGnt FAIL
```

In this example, we removed the action block associated with the true (i.e. pass) evaluation of the property to avoid the vacuous \$display.

If you do need an action block for a match (i.e. Pass) of a property, you may use a 'cover' statement to cover the same property that is asserted.

The simulators that the author have tried do filter out vacuous pass on a 'cover', giving you only a Pass indication when antecedent is True and Consequent matches.

Concurrent Assertion - with 'cover'... take 2...

OK, what if your simulator does not filter for a vacuous pass on a 'cover'.

There are many ways to get around it. Here's one. 'cover' the sequence/property -without- an implication.

```
property pr1;  
    @(posedge clk) req |-> ##2 gnt;  
endproperty
```

```
property pr2;  
    @(posedge clk) req ##2 gnt;  
endproperty
```

No action_block associated with true eval of the property.

```
A_reqGnt: assert property (pr1) else $display($stime,, "\t\t %m FAIL");  
C_reqGnt: cover property (pr2) $display($stime,, "\t\t %m PASS");
```

```
# run -all  
#    10 clk=1 req=0 gnt=0  
#    30 clk=1 req=1 gnt=0  
#    50 clk=1 req=0 gnt=0  
#    70 clk=1 req=0 gnt=1  
#    70      test_basic_property2.C_reqGnt PASS  
#    90 clk=1 req=1 gnt=0  
#   110 clk=1 req=0 gnt=0  
#   130 clk=1 req=0 gnt=0  
#   130      test_basic_property2.A_reqGnt FAIL
```

For 'cover' we removed the implication operator. Vacuous pass applies only when there is an implication operator and the antecedent does not match.

Without an implication operator there is no vacuous pass and since there is no 'failure' action_block with a 'cover' you get a pass indication only when the property/sequence matches...

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Thomas Slee, Sr. Electrical Engineer, ASIC Verification Lead, Space System Loral

"The seminar on SVA was very educative and informative. The material was in-depth, was from a hardware design/verification person's perspective and it was vendor neutral. The information was very good and I hope to have a chance to use it in the future."

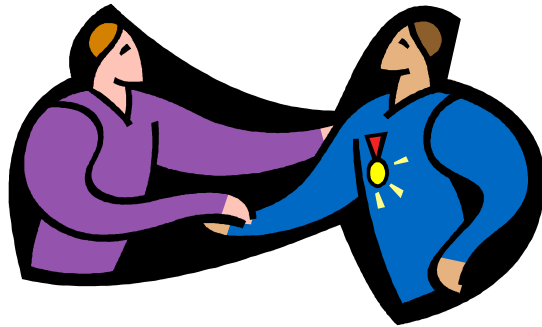
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happy asserting...

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