‘concurrent assertion’

it’s a vacuous world !

Concurrent Assertion – *without* an implication

Look! NO IMPLICATION

```
property pr1;
  @(posedge clk)  req ##2 gnt;
endproperty

reqGnt: assert property (pr1)   $display($stime,,,"\t\t %m PASS");  else
                                $display($stime,,,"\t\t %m FAIL");
```

Simulation Log

```
# run -all
#         10  clk=1 req=0 gnt=0
#         10            test_basic_property.reqGnt FAIL
#         30  clk=1 req=0 gnt=0
#         30            test_basic_property.reqGnt FAIL
#         50  clk=1 req=1 gnt=0
#         70  clk=1 req=0 gnt=0
#         70            test_basic_property.reqGnt FAIL
#         90  clk=1 req=0 gnt=1
#         90            test_basic_property.reqGnt FAIL
#         90            test_basic_property.reqGnt PASS
#        110  clk=1 req=0 gnt=0
#        110            test_basic_property.reqGnt FAIL
```

Whenever 'req' is Low, the assertion FAILs !!

That's because, a sequence simply says that 'req' be true at the clock edge and that gnt must be true 2 clocks later.

It does **NOT** say check the sequence "Only *If* 'req' is true at posedge clk".

But you really don't care for result when 'req' is Low.

That's where an implication operator comes into picture…

Concurrent Assertion – *with* an implication

```
sequence sr1;
  ##2 gnt;
endsequence

property pr1;
        @(posedge clk) req  |->  sr1;
endproperty

reqGnt: assert property (pr1)   $display($stime,,,"\t\t %m PASS");  else
                                $display($stime,,,"\t\t %m FAIL");
```

IMPLICATION OPERATOR (OVERLAPPING)

ANTECEDENT

CONSEQUENT

Simulation Log

```
#        10  clk=1   req=0 gnt=0
#        10          test_basic_property1.reqGnt PASS
#        30  clk=1   req=1 gnt=0
#        50  clk=1   req=0 gnt=0
#        50          test_basic_property1.reqGnt PASS
#        70  clk=1   req=0 gnt=1
#        70          test_basic_property1.reqGnt PASS
#        70          test_basic_property1.reqGnt PASS
#        90  clk=1   req=1 gnt=0
#       110  clk=1   req=0 gnt=0
#       110          test_basic_property1.reqGnt PASS
#       130  clk=1   req=0 gnt=0
#       130          test_basic_property1.reqGnt FAIL
```

In this example, we moved a part of the sequence to the property and are using it as an antecedent to imply a consequent.

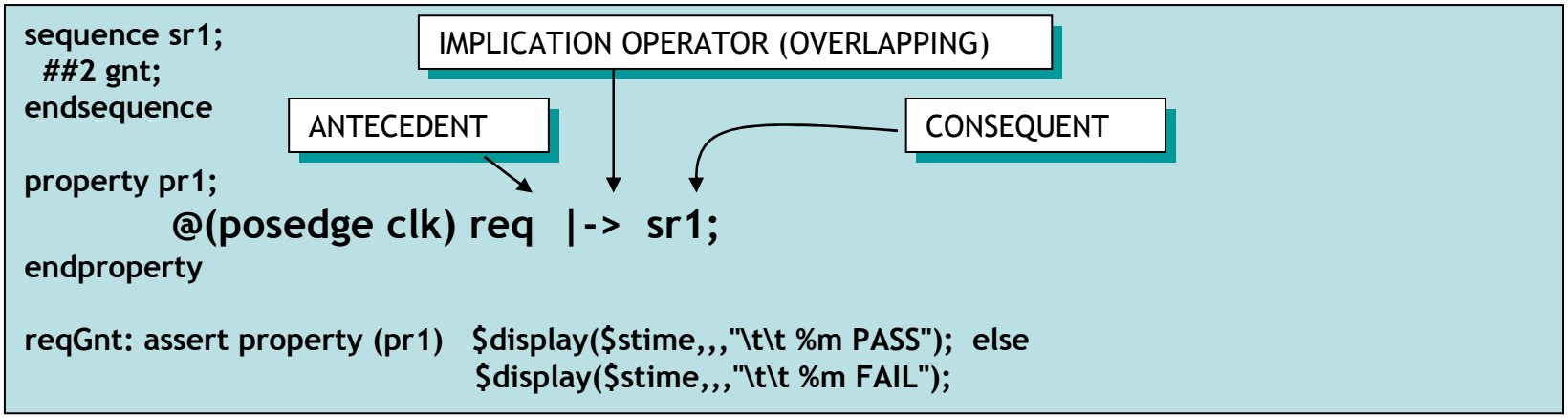
With an implication operator, the 'antecedent' MUST be TRUE to evaluate the consequent. Hence, whenever 'req' is Low, the antecedent is false and the implication simply does not fire and there is no failure message as in the previous example.

BUT WAIT…

Now the property PASSes whenever 'req' is Low.

What's going on???

Concurrent Assertion – *Vacuous Pass – What ??*



LRM 3.1a (Page 232) ::

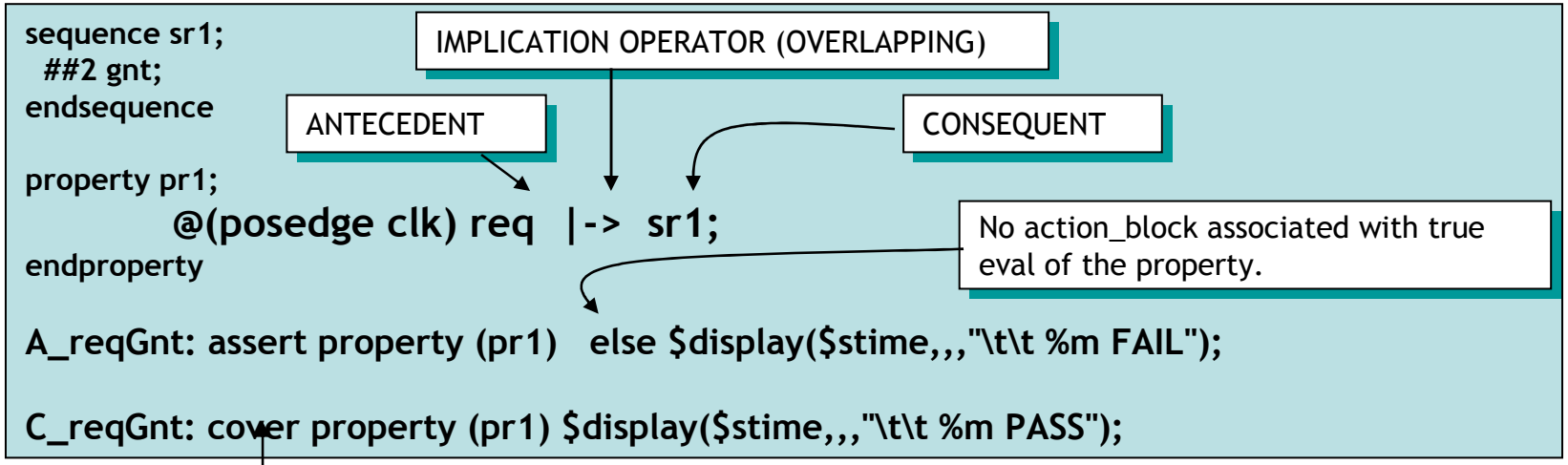
"If there is no match of the antecedent sequence_expr, then evaluation of the implication succeeds vacuously and returns true"

A couple of ways to get around this…

One is to simply not use the action_block associated with 'pass' (duh…) of the property, so that you don't get pass indication vacuously

But what if you do want to know when the property passes…

Concurrent Assertion – with 'cover'… take 1…



You may use a 'cover' statement to cover the same property that is asserted. 'cover' does not report vacuous pass ***(but note that many simulators require a run time option to 'filter' out vacuous pass on a 'cover')***.

Note that 'cover' does not allow an action_block if the property fails.

```
# run -all
#        10  clk=1   req=0 gnt=0
#        30  clk=1   req=1 gnt=0
#        50  clk=1   req=0 gnt=0
#        70  clk=1   req=0 gnt=1
#        70          test_basic_property2.C_reqGnt PASS
#        90  clk=1   req=1 gnt=0
#       110  clk=1   req=0 gnt=0
#       130  clk=1   req=0 gnt=0
#       130          test_basic_property2.A_reqGnt FAIL
```

In this example, we removed the action block associated with the true (i.e. pass) evaluation of the property to avoid the vacuous $display.

If you do need an action block for a match (i.e. Pass) of a property, you may use a 'cover' statement to cover the same property that is asserted.

The simulators that the author have tried do filter out vacuous pass on a 'cover', giving you only a Pass indication when antecedent is True and Consequent matches.

Concurrent Assertion – with 'cover'… take 2…

OK, what if your simulator does not filter for a vacuous pass on a 'cover'.

There are many ways to get around it. Here's one. 'cover' the sequence/property -without- an implication.

```
property pr1;
        @(posedge clk) req  |->  ##2 gnt;
endproperty

property pr2;
        @(posedge clk) req ##2 gnt;
endproperty

A_reqGnt: assert property (pr1)  else $display($stime,,,"\t\t %m FAIL");
C_reqGnt: cover property (pr2) $display($stime,,,"\t\t %m PASS");
```

No action_block associated with true eval of the property.

```
# run -all
#        10  clk=1   req=0 gnt=0
#        30  clk=1   req=1 gnt=0
#        50  clk=1   req=0 gnt=0
#        70  clk=1   req=0 gnt=1
#        70            test_basic_property2.C_reqGnt PASS
#        90  clk=1   req=1 gnt=0
#       110  clk=1   req=0 gnt=0
#       130  clk=1   req=0 gnt=0
#       130            test_basic_property2.A_reqGnt FAIL
```

For 'cover' we removed the implication operator. Vacuous pass applies only when there is an implication operator and the antecedent does not match.

Without an implication operator there is no vacuos pass and since there is no 'failure' action_block with a 'cover' you get a pass indication only when the property/sequence matches…

DefineView Consulting

DefineView Consulting offers comprehensive trainings and consulting services in

System Verilog Assertions and Functional Coverage

that go into in-depth detail of such language nuances with simple to understand examples and real life applications. Taught from and end user point of view, the training also includes practical LABs to put it all in perspective.

1 Day Training in System Verilog Assertions Language and Methodology with LABs

2 Day Training in System Verilog Assertions & Functional Coverage Language and Methodology with many more LABs and applications.

Please visit http://defineview.com/trainingpricing for complete detail on both these classes.

CUSTOMER TESTIMONIALS …

"Ashok is a very good instructor - very impressive."

John Reykjalin, President, Grizzly Peak Engineering, Inc.

"The class was excellent, well distributed between the fundamentals and the practical examples. With a little tweak, we can use those example assertions presented right now in our design development! In addition I would like to thank you for seminar associated text material. The handout (book) is a few levels above anything I have previously seen. The rules and example descriptions cover the associated topic completely."

Thomas Slee, Sr. Electrical Engineer, ASIC Verification Lead, Space System Loral

"The seminar on SVA was very educative and informative. The material was in-depth, was from a hardware design/verification person's perspective and it was vendor neutral. The information was very good and I hope to have a chance to use it in the future."

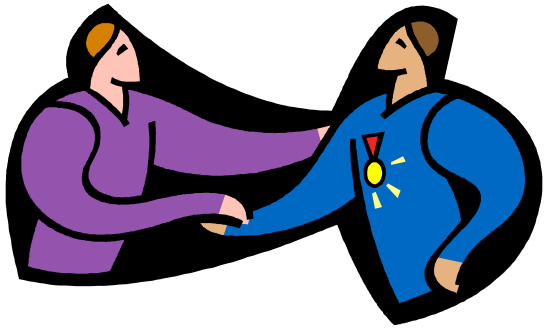
Shubha Umesh, Senior Logic Engineer, LeCroy Corporation

"I like the seminar very much since it's packed full of technical explanations and examples of System Verilog Assertion. You slides are also easy to follow and understand."

Gloria Chen, ASIC Verification Engineer, 3PAR

"Your seminar clearly showed us that System Verilog Assertions provide new powerful interfaces and how they are implemented as part of the language. Your seminar was one of the best seminar I ever had."

Aki Niimura-san, Ponderosa Design



happy asserting…

For a detailed training that takes you through System Verilog Assertions and Functional Coverage language and methodology step by step with examples/simulation logs, real life applications and practical LABs please contact…

DefineView Consulting
www.defineview.com

(email) ashok@defineview.com
(phone) 408.309.1556