SystemVerilog Assertions

Language and Methodology

Training Agenda

(1 Day Class with 3 LABs)

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Training :: Abstract

- **What is SVA (SystemVerilog Assertions)**
  - SystemVerilog Assertions (SVA) is a powerful subset of the IEEE 1800 SystemVerilog standard.
  - Its hardware oriented concurrent semantics allow for intuitive development of complex multi-clock domain assertions to catch those elusive bugs at the source.
  - SVA works both with VHDL and Verilog. Clean separation between RTL design and SVA assertions.
  - Parameterized reusability.

- **Course Highlights**
  - Each operator/feature is explained in detail using comprehensive examples, timing diagrams and simulation logs.
  - Real life applications are discussed to put it all in perspective.
  - A reference grade handout book is provided to the class. It has comprehensive detail on each page that can serve as excellent reference material for future.
  - Labs are geared to solidify understanding of key concepts using application oriented designs.

Training :: Agenda

- **Introduction to Assertions**
  - What's an assertion? Why can't I just use Verilog?
  - Advantages of Assertion Based Verification (ABV) .
  - Assertion Based Verification (ABV) Methodology components
- **System Verilog Assertions :: Syntax and Semantics (with applications)**
  - Immediate assertions
  - Concurrent assertions - Basics
    - clocking basics; formal arguments; severity levels; threads
    - Sequence introduction
    - Property introduction (with/without an implication)
    - Vacuous pass?
    - Binding properties.
    - Threading (*what are the performance implications*?)
  - Sampled value functions (in property/sequence and procedural)
    - Functions that return Boolean pass/fail: $rose, $fell, $stable
    - Function that return sampled value; $past (with/without gating expr.)
  - Sequence Operators
    - ##m and ##[m:n] clock delay (*SVA allows only fixed delays. So what if you want variable delays??)*
    - [*] and [*m:n] – Consecutive repetition operator
    - [=] and [=m:n] – Non-consecutive repetition operator
    - [->] and [-> m:n] – Goto (non-consecutive) repetition operator
    - Pros/Cons of infinite ($) range
    - 'throughout', 'within', 'intersect', 'first_match'
    - 'and' and 'or' of sequences with/without delay range
    - 'intersect' vs. 'and'

Training :: Agenda (contd.)

- Property operators
  - 'not' operator; If … else ; 'disable iff'
- Recursive property
  - Mutually exclusive, 0 delay infinite loop, Restrictions
- System functions
  - $onehot, $onehot0, $isunknown, $countones
- Multiple Clocks / Multiply clocked properties and sequences
- Local variables (one of the most powerful features...)
  - Pipelined behavior (multiple threads)
- Detecting and using endpoint of a sequence
  - .ended, .matched, .triggered

- **LABs**
  - LAB 1: Learn how to 'bind' property module with design module.
    - Understand vacuous pass and properties with/without implication
  - LAB 2: Enforces how pipelined threads of a property work.
  - LAB 3: Synchronous FIFO
    - A synchronous FIFO design is presented. You will write assertions to check for various FIFO fail conditions.
    - FIFO assertions are some of the most useful assertions to write for any design. The assertions developed in this LAB will be directly applicable to your design.

CUSTOMER TESTIMONIALS …

"Ashok is a very good instructor – very impressive."

John Reykjalin, President, Grizzly Peak Engineering, Inc.

"The class was excellent, well distributed between the fundamentals and the practical examples. With a little tweak, we can use those example assertions presented right now in our design development!
In addition I would like to thank you for seminar associated text material. The handout (book) is a few levels above anything I have previously seen. The rules and example descriptions cover the associated topic completely."

Thomas Slee, Sr. Electrical Engineer, ASIC Verification Lead, Space System Loral

"The seminar on SVA was very educative and informative.
The material was in-depth, was from a hardware design/verification person's perspective and it was vendor neutral. The information was very good and I hope to have a chance to use it in the future."

Shubha Umesh, Senior Logic Engineer, LeCroy Corporation

"Ashok, I take this opportunity to personally thank you for your dedication. You have very good knowledge on the subject. I intend to now use assertions heavily on my next verification project and will use your examples extensively. This class helped me strengthen my knowledge on SVA."

Mohammad Ashraf, Sr. Electrical Engineer, Space System LORAL

Ashok Mehta

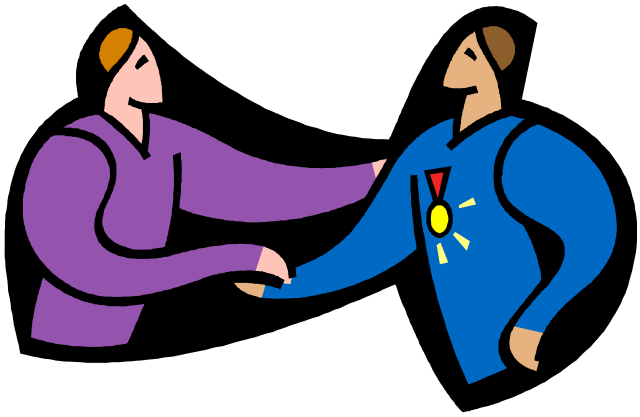
INTRODUCTION

- **30+ years of experience in SoC, CPU design and verification**
- **Author of two books**
  - SystemVerilog Assertions and Functional Coverage (2nd edition - 2016)
    - 400+ pages
  - ASIC/SoC Functional Design Verification (2018)
    - 320+ pages
- **17 US Patents on 3DIC and SoC verification**

CURRENT ACTIVITIES

- **Verification Methodology Adviser to FPGA, SoC and Systems companies.**
  - Methodology evaluation; creation; customization
- **SVA and Functional Coverage Training**
  - Customized to your requirements
- **SVA and FC Training class on UDEMY**
  - 33 lectures; 8.5 hours; life time access; in-depth from scratch

happy asserting…



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