DefineView Consulting

Expert Training, Verification Methodology Advisory

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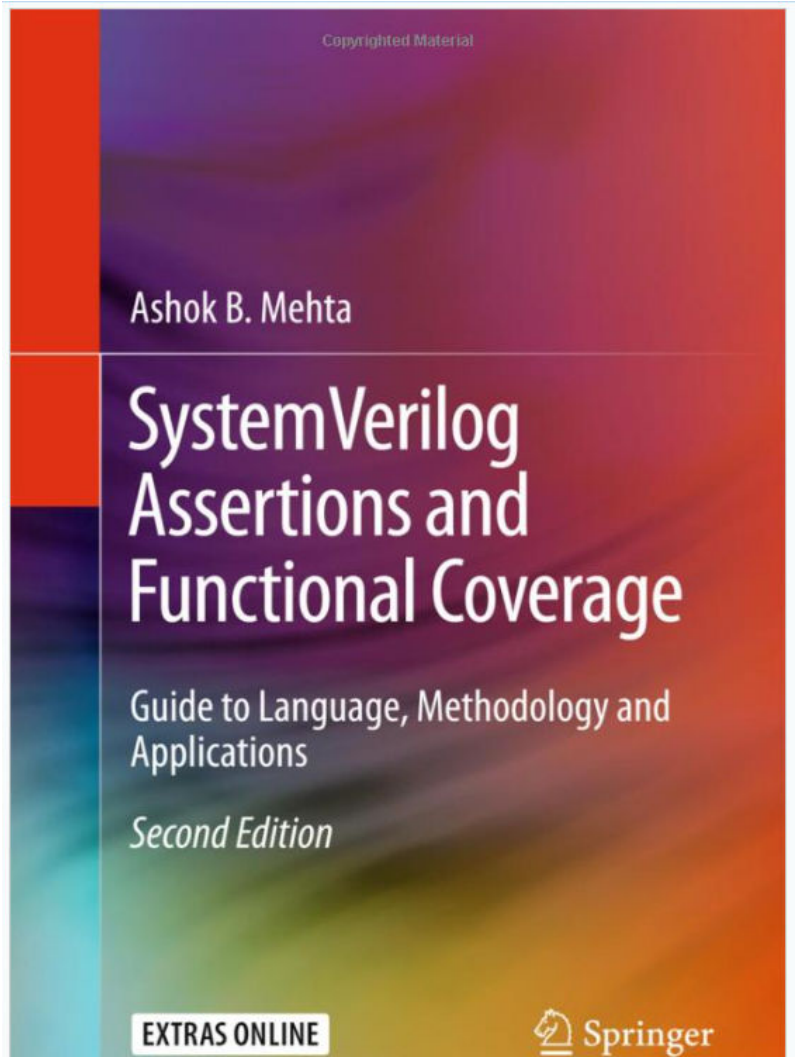
Ashok Mehta

- 30+ years of experience in SoC, CPU design and verification at DEC, Data General, Intel, Applied Micro, TSMC
- Author of two books
  - SystemVerilog Assertions and Functional Coverage (2nd edition)
    - A comprehensive guide to languages, methodology and applications
  - ASIC/SoC Functional Design Verification
    - A comprehensive guide to technologies and methodologies
- 17 US Patents on 3DIC and SoC verification
- Expertise in:
  - Coverage Driven Verification (CDV)
  - Assertion Based Verification (ABV)
  - Universal Verification Methodology (UVM)
  - Constrained Random Verification (CRV)
  - Behavioral/Architectural modeling in Verilog
  - Static Formal verification
  - Hardware Acceleration,
  - ESL/Virtual Platform (TLM 2.0), etc.

Ashok Mehta – 17 issued US Patents

Subject matter of the patents is Design Verification of SoC, 2.5D IC and 3DIC (i.e. verifying stacked dies). Also, progressive reusable refinement of Verification from Algorithm to RTL level. Simulating RTL with TLM2.0 ESL Models.

	PAT. NO.		Title
1	9,646,128	T	System and method for validating stacked dies by comparing connections
2	9,625,971	T	System and method of adaptive voltage frequency scaling
3	9,612,277	T	System and method for functional verification of multi-die 3D ICs
4	9,552,448	T	Method and apparatus for electronic system model generation
5	9,514,268	T	Interposer defect coverage metric and method to maximize the same
6	9,404,971	T	Circuit and method for monolithic stacked integrated circuit testing
7	9,158,881	T	Interposer defect coverage metric and method to maximize the same
8	9,110,136	T	Circuit and method for monolithic stacked integrated circuit testing
9	9,047,432	T	System and method for validating stacked dies by comparing connections
10	9,015,649	T	Method and apparatus for electronic system model generation
11	8,972,918	T	System and method for functional verification of multi-die 3D ICs
12	8,966,419	T	System and method for testing stacked dies
13	8,826,202	T	Reducing design verification time while maximizing system functional coverage
14	8,578,309	T	Format conversion from value change dump (VCD) to universal verification methodology (UVM)
15	8,522,177	T	Method and apparatus for electronic system function verification at two levels
16	8,402,404	T	Stacked die interconnect validation
17	8,336,009	T	Method and apparatus for electronic system function verification at two levels



This book provides a hands-on, application-oriented guide to the language and methodology of both SystemVerilog Assertions and SystemVerilog Functional Coverage.

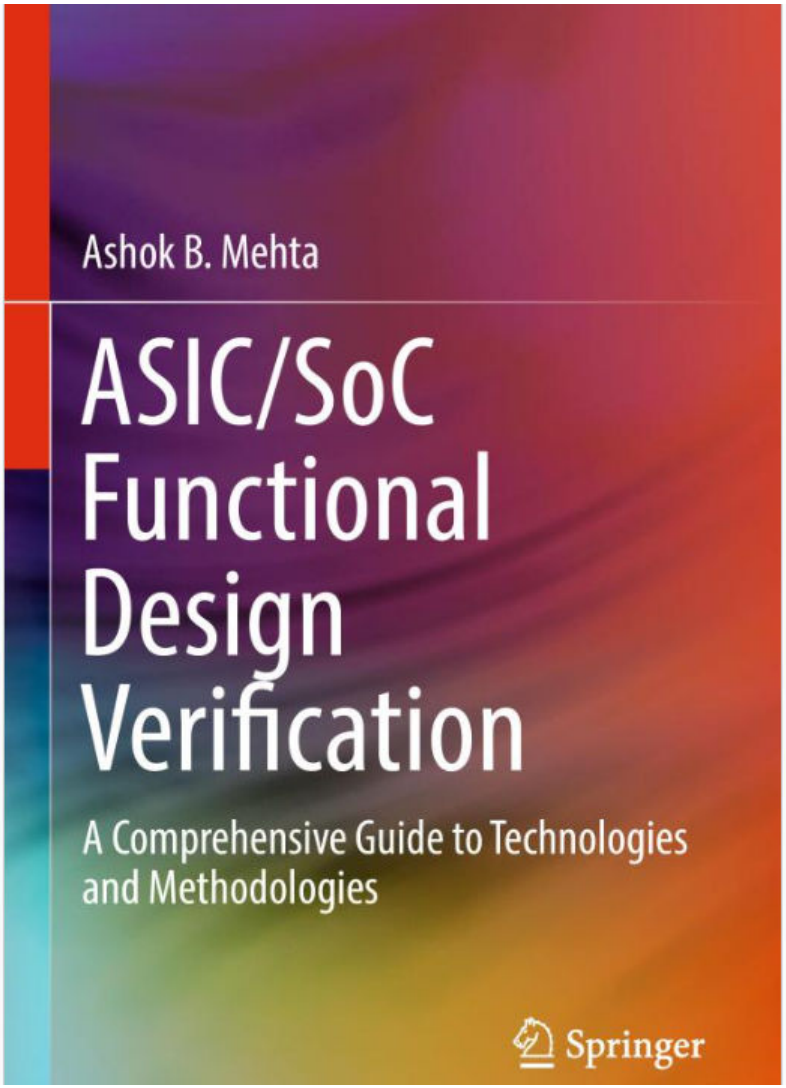
Readers will benefit from step-by-step approach to functional hardware verification using SystemVerilog Assertions and Functional Coverage.

The book has a strong end-user perspective, which makes it plenty easy to digest complex features and apply them with ease to a design.

Plenty of real-life applications

This is an excellent Reference Book

The book will enable design verification engineers to uncover hidden and hard to find bugs, point directly to the source of the bug, provide for a clean and easy way to model complex timing checks and objectively answer the question ‘have we functionally verified everything’.



This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment.

The author describes industry standard technologies such as

UVM (Universal Verification Methodology)

SVA (SystemVerilog Assertions)

SFC (SystemVerilog Functional Coverage)

CDV (Coverage Driven Verification)

Low Power Verification (Unified Power Format UPF)

AMS (Analog Mixed Signal) verification

Virtual Platform TLM2.0/ESL (Electronic System Level) methodology

Static Formal Verification

LEC (Logic Equivalency Check)

Hardware Acceleration

Hardware Emulation, Hardware/Software Co-verification

PPA (Power Performance Area) analysis on a virtual platform

Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies

Ashok Mehta – current activities

- **ASIC/FPGA/SoC Verification methodology review and technical guidance on building efficient, reusable Verification Methodology: *Customized to your Design***
  - **Coverage Driven Verification (CDV)**
  - **Assertion Based Verification (ABV)**
  - **Coverage Methodology (Code, Functional, Sequential Logic)**
  - **Universal Verification Methodology (UVM)**
  - **Constrained Random Verification**
  - **Behavioral (modular, reusable) Testbench Methodology in Verilog**
  - **Static Formal verification**
- **Expert training in SystemVerilog Assertions and Functional Coverage: *Customized to your requirements***
- **Technical guidance on deployment of SystemVerilog Assertions and Functional Coverage Methodology.**
  - **SVA and FC adoption does *not* require knowledge of UVM or SystemVerilog.**
- **Hands-on development of SVA Assertions and Functional Coverage (Covergroups, Coverpoints, etc.)**
- **System Level Virtual Platform (TLM 2.0) development guidance for Test Generation and Software Development.**

Watch out Design bugs…

Please visit our web site for further detail…

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